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a second portion being less resistant to breakdown, the second portion comprising a diode, wherein the diode has an identical structure as the MOS transistor, except for a source region.

REMARKS

Claims 1-3, 6-9, and 15-16 are pending. By this amendment, claims 4 and 5 have been cancelled and claim 1 has been amended. Reconsideration and allowance are respectfully requested in view of the above amendments and the following remarks. No new matter is believed added.

Claims 1-4 and 6 are rejected under 35 U.S.C. §102(b) as being anticipated by Momose et al. (US 5,990,516), hereafter "Momose." Claims 1-6 are rejected under 35 U.S.C. §102(e) as being anticipated by Letavic et al. (US 6,133,591), hereafter "Letavic '591." Claims 1-4 and 6 are rejected under 35 U.S.C. §102(e) as being anticipated by Kouno et al. (US 6,365,932), hereafter "Kouno." Claims 1-4 and 6 are rejected under 35 U.S.C. §102(e) as being anticipated by Kamei et al. (JP 2000-260883), hereafter "Kamei." Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kamei in view of Letavic et al. (US 5,969,387), hereafter "Letavic '387." Claims 7 and 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Letavic '591 in view of Honda et al. (US 5,834,823), hereafter "Honda." Claims 7 and 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kouno in view of Honda. Claims 7 and 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kouno in view of Pendharkar et al. (US 6,160,290), hereafter "Pendharkar." Claim 15 is rejected under 35 U.S.C.

§103(a) as being unpatentable over Letavic '591 in view of Honda. Claims 15-16 are rejected under 35 U.S.C. §103(a) as being unpatentable over Letavic '387 in view of Honda. Claims 15 and 16 are rejected under 35 U.S.C. §103(a) as being unpatentable over Letavic '387 in view of Pendharkar.

The above-referenced rejections are defective because the references, taken alone or in any combination, fail to teach or suggest each and every feature of the claimed invention as required by 35 U.S.C. §102 and §103.

Claim 1 sets forth a hybrid semiconductor device that includes a first portion being relatively resistant to breakdown, the first portion comprising a MOS transistor; and a second portion being less resistant to breakdown, the second portion comprising a diode, wherein **the diode has an identical structure as the MOS transistor, except for a source region**. None of the references cited by the Examiner, taken alone or in combination, teach or suggest such a hybrid semiconductor device.

In sections 4 and 8 of the Office Action, the Examiner asserts that Letavic '591 and Letavic '387 teach the claimed "diode (see fig. 3) having an identical structure as the MOS transistor, except for a source region." Applicants respectfully disagree with the Examiner's analysis of these references.

Letavic '591 discloses (see, e.g., col. 2, lines 27-31, col. 4, lines 27-51) an SOI hybrid transistor device structure including at least one MOS transistor structure segment and, as shown in FIG. 3, at least one **conductivity modulation transistor structure segment** (e.g., a LIGB transistor structure). Further, the structure of the conductivity modulation transistor structure

segment (FIG. 3) is not identical to the structure of the MOS transistor structure segment (FIG. 2) “except for a source region.” For example, Letavic ‘591 discloses that the drain region 34 (FIG. 2) is replaced with an anode region 40 (FIG. 3) that “should not extend at its left side to contact the oxide region 38b, as in FIG. 2, but rather should be spaced apart from this region” (col. 4, lines 37-47). Clearly, Letavic ‘591 does not disclose a **diode** having an identical structure as the MOS transistor, except for a source region as claimed.

Letavic ‘387 discloses a lateral thin film SOI device such as a MOSFET (FIG. 1) **or** a diode (FIG. 3). Letavic ‘387 does not disclose a hybrid device containing both a MOS transistor **and** a diode. Moreover, the diode structure illustrated in FIG. 3 of Letavic ‘387 is not identical to the MOSFET structure illustrated in FIG. 1 Letavic ‘387, “except for a source region..” For example, in FIG. 1, the portion 114a of the conductive field plate 114 is insulated from first region 106 by a layer of oxide 112a. In FIG. 3, however, the portion 114b of the conductive field plate 114 directly contacts first region 106. Clearly, Letavic ‘387 does not disclose a diode having an identical structure as the MOS transistor, except for a source region as claimed.

Claim 15 sets forth a hybrid lateral thin-film SOI device that includes first and second regions, wherein the second regions are “identical to the first region, except not comprising said source region, and having a field plate of shorter length than that of the first regions.” None of the references cited by the Examiner, taken alone or in combination, teach or suggest such a hybrid lateral thin-film SOI device.

In section 14 of the Office Action, the Examiner asserts that Letavic ‘591 teaches first and second regions, wherein the second regions are “identical to the first regions, except not

comprising said source regions (see fig. 3). Applicants respectfully disagree with the Examiner's analysis of this reference. In particular, in Letavic '591, the structure of the conductivity modulation transistor structure segment (FIG. 3) is not identical to the structure of the MOS transistor structure segment (FIG. 2) "except for a source region." On the contrary, Letavic '591 discloses that the drain region 34 (FIG. 2) is replaced with an anode region 40 (FIG. 3) that "should not extend at its left side to contact the oxide region 38b, as in FIG. 2, but rather should be spaced apart from this region" (col. 4, lines 37-47).

Accordingly, in view of the foregoing, Applicants respectfully submit that claims 1-3, 6-9, and 15-16 are allowable.

If the Examiner believes that anything further is necessary to place the application in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number listed below.

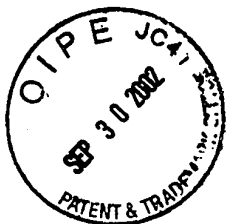
Dated: 9/25/02

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Applicant: Petruzzello et al.

Application No.: 09/894,083

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For: HV-SOI LDMOS DEVICE WITH
INTEGRATED DIODE TO IMPROVE
RELIABILITY AND AVALANCHE
RUGGEDNESS

Examiner: Sefer, A.

Art Unit: 2826

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SEPARATE MARKUP SHEET

IN THE CLAIMS

Please amend claim 1 to appear as set forth below. The changes made thereto are shown in the attached Separate Markup Sheet.

1. (Amended) A hybrid semiconductor device, comprising:

a first portion being relatively resistant to breakdown, the first portion comprising a MOS transistor; and

a second portion being less resistant to breakdown, the second portion comprising a diode, wherein the diode has an identical structure as the MOS transistor, except for a source region.